Design of An Effective, Low Power and less complex 6 bit flash ADC using CMOS

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Abstract: Different electronic devices such as mobile phones, DSPs, etc., are designed by using VLSI (Very Large Scale Integration) technology. In VLSI dynamic CMOS logic circuits are concentrating on the reducing the Power consumption, Area (portability of the system), and increasing the Speed by reducing the delay. In this paper , a new design for flash ADC is discussed . The architecture enables power reduction using CMOS technology .Digital signals play phenomenal role in effective power utilization .Designs like Wilkinson type ADC, Counter ADC exist , and they do not have power efficiency .Here tools like Mentor Graphics Tanner , Microwind are used .

Keywords:- Flash ADC, Low power ADC , CMOS comparators.

I. INTRODUCTION

Most of the digital circuit involves focus on Analog to Digital communication . The speed of the conversion , the circuitry and the power consumed in the design should be taken into consideration while the designs are made .The ultimate goal of any circuit is to be made with less circuitry and low power consumption .The conversion speed (the number bits converted into the digital from analog per second) should be maximized for any design . Based on the structural observations of comparators in digital circuits , the flash ADCs have been classified in to series and parallel architecture .In general Parallel flash ADC have more conversion rate and are used for pragmatic purpose. The proposed architecture emphasizes on reduction of the circuitry with less power consumption .

II. CONVENTIONAL FLASH ADC

The existing flash ADC architecture is shown in figure 1.In general for a n bit flash ADC ,it requires 2^n-1 comparators . So , for a 6 bit flash ADC , we require 63 comparators .Though the conversion speed in higher , the circuit complexity is more . Here the circuit looks clumsy just for a 6 bit flash Adc , and if the Adc is to made for higher no of bits , the circuit gets more complicated . This results in more power consumption and low power circuitry .

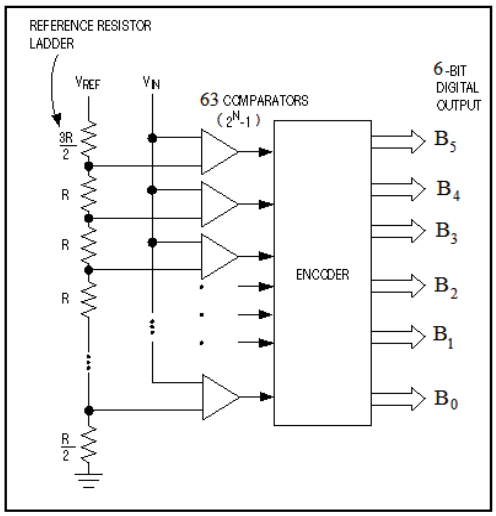


figure1:conventional and existing flash ADC.

The proposed architecture is presented below .

III. Proposed Flash ADC architecture

In this we implement the architecture using 9 multiplexers and 10 comparators . In this architecture the time taken to produce the output are almost same and hence emphasis is done on the power consumption part .The speed is same here because the comparator we are making is almost similar to the parallel architecture .

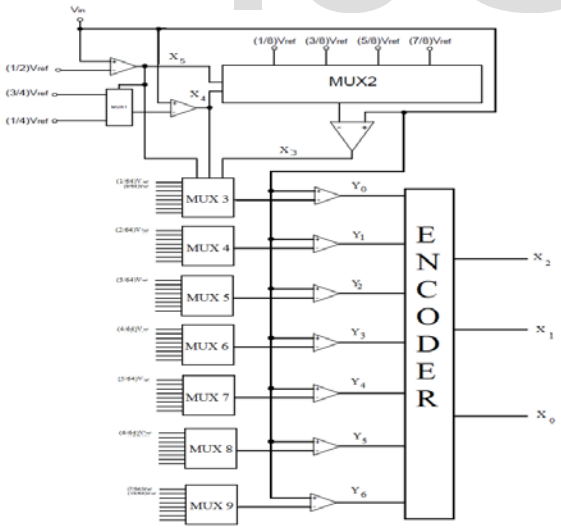


figure 2: Proposed architecture

The 6 bit output are here denoted by X0,X1,X2,X3,X4,X5,X6 . Multiplexers contain generally multiple inputs and one output . By using the multiplexers , the circuit complexity can be reduced to a lot extent .The outputs X3,X4,X5 are used indirectly for obtaining values of X0,X1,X2 . The various voltages (VREF) are applied based on the requirement in the circuit .

Here the comparator can be constructed using the CMOS technology . Here the output of CMOS is fed into the input of S-R latch .The same is shown in figure 3

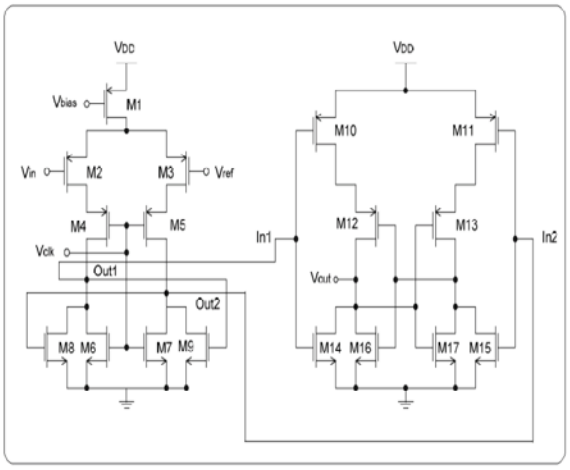
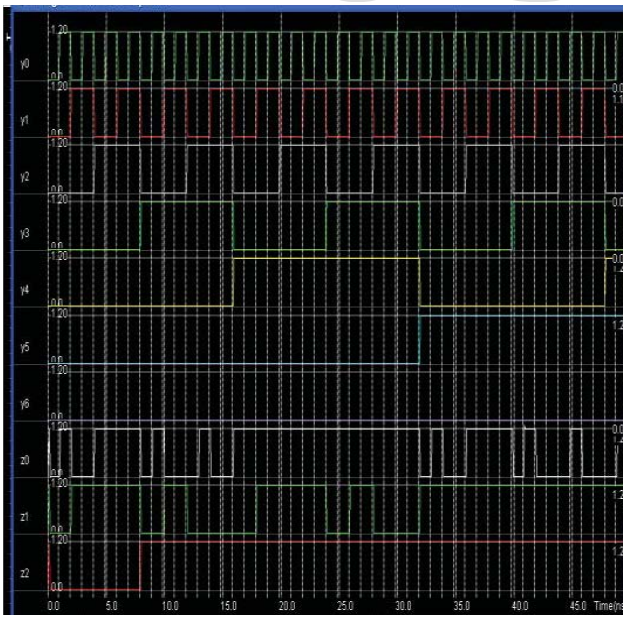


figure 3:comparator made with CMOS and SR latch .

IV.SIMULATION RESULTS

The results are obtained using the Tanner software .The figure 4 shows the simulation result containing the voltage vs time plot for the encoder part .



From the simulation results ,the following power consumption values are obtained .The following table shows the power consumption for the proposed method :

No of units	Component name	Individual component (in uW)	Total power consumed by each component(in uW)
7	8X1 Mux	42	294
1	2X1 Mux	18.2	18.2
10	comparator	40.5	405
1	encoder	17.35	17.35
		TOTAL POWER CONSUMED =	734.55

Similarly , the following table shows the power consumption in the convention method :

No of units	Component name	Individual component (in uW)	Total power consumed by each component(in uW)
63	Comparator	39.25	2472.75
1	Encoder	92.67	92.67
		Total Power consumed =	2565.42

From the tables listed we have clear picture of the power consumed in the existing and the proposed architecture .We can state that the power consumed in the proposed architecture is far less compared to the existing conventional architectures . Finally , we can state that the proposed one is superior to the present ones .

V CONCLUSION :

Here ,a new architecture is proposed and the same is implemented which has better performance in terms of the power consumption and the circuit complexity

. The same can be implemented in different nm technology and various clock speeds . Further the architecture can be improved by placing transmission gates at the place of encoder which has very less delays compared to others .

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